Comments on "Improved Accuracy Pseudo-Exponential Function Generator With Applications in Analog Signal Processing"

Neha V. Karanjkar, Rasmi R. Sahoo, and Maryam Shojaei Baghini

***Abstract*—Recently a new CMOS current-mode pseudo-exponential function generator circuit was reported by Popa. The entire analysis and exponential function generator circuit, given in Popa's paper, is based on a current-squaring circuit module. In this comment paper we show that the current-squarer circuit, presented in Popa's paper, does not work as a current squarer. Consequently the pseudo-exponential generator also does not work as described in Popa's paper. We present a detailed mathematical analysis in this paper to derive its actual operation. Simulation results of the circuit module using Mentor Graphics custom IC design tool set, in a TSMC 0.18-μm CMOS process, are also shown in this paper. Simulation results match the behavior predicted by mathematical analysis.**

***Index Terms*—Analog signal processing, CMOS analog integrated circuits, current-squaring circuit.**

I. Introduction

A new CMOS current-mode pseudo-exponential function generator has been reported recently in [1]. The entire analysis and exponential function generator circuit given in [1] is based on a current-squaring circuit (given in Fig. 1 of the same paper). The schematic of current-squaring circuit is reproduced in this paper in Fig. 1. The current-squaring circuit takes two *independent* input currents $I_{\rm IN}$ and $I_{\rm O}$, and is intended to produce an output current $I_{\rm OUT}$ equal to $I_{\rm IN}^2/I_{\rm O}$.

In this comment paper we show that the circuit for the current-squarer module presented in [1] is incorrect. We show a proper input-output (I/O) arrangement for this circuit, and prove that even with a proper I/O arrangement, the circuit has a fundamental problem: it produces $I_{\rm OUT}$ equal to $I_{\rm IN}^2/I_{\rm O}$, *only* if $I_{\rm IN}$ and $I_{\rm O}$ are *quadratically related*. In essence, the circuit never works as a current squarer for independent values of $I_{\rm IN}$ and $I_{\rm O}$. Consequently, the pseudo-exponential function generator presented in [1], which uses the current-squaring circuit as a building block, does not work correctly. To support the argument, simulation results of the current-squaring circuit reported in [1], current-squarer module with proper I/O arrangement, and the pseudo-exponential generator are shown in this paper. All simulations are done using TSMC 0.18-μm process model files in the Mentor Graphics custom IC design environment.

For ease of comparison, the same notations as those of [1] are used in this paper.

II. Analysis of the Current-Squarer Circuit

Consider the current-squarer circuit given in Fig. 1. $I_{\rm IN}$ and $I_{\rm O}$ are two independent input currents and $I_{\rm OUT}$ is the output current. The circuit has the following errors.

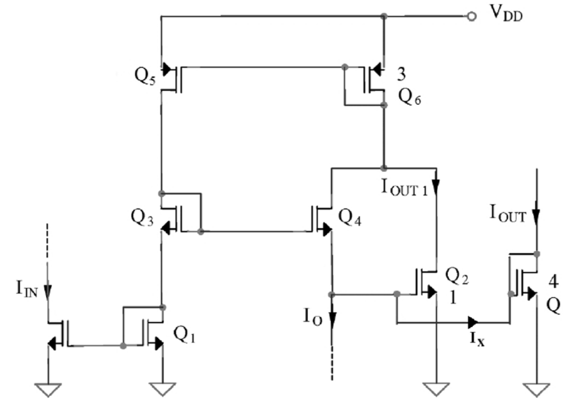

Fig. 1. CMOS current-squaring circuit as presented in [1].

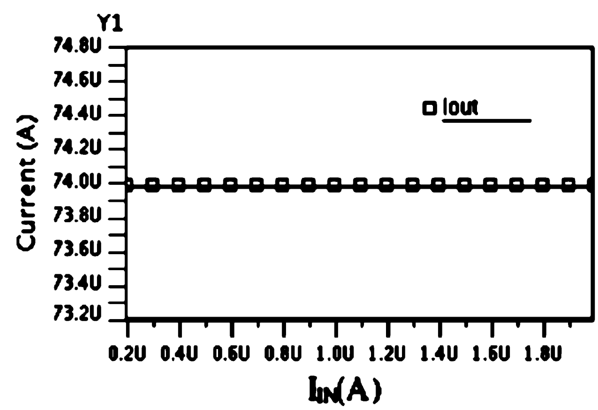

Fig. 2. Simulation results of the current-squaring circuit shown in Fig. 1.

1) Gate voltage of Q_1 will not vary with $I_{\rm IN}$ as there is no feedback from drain to gate in the input transistor. The input transistor needs to be diode-connected for correct operation of the current mirror.
2) It is stated in [1, Sec. II-A] that $I_{\rm O} + I_{\rm OUT1} = 3I_{\rm IN}$. However it can be seen from Fig. 1 that Q_7 is diode-connected, and hence $I_{\rm O} + I_{\rm X} + I_{\rm OUT1} = 3I_{\rm IN}$ where $I_{\rm X} = I_7 - I_{\rm OUT}$.

Fig. 2 shows the simulation results of the circuit shown in Fig. 1. $I_{\rm OUT}$ does not vary with $I_{\rm IN}$. Fig. 3 shows the current-squarer circuit modified to provide proper I/O arrangement.

III. Theoretical Analysis

Consider the current-squarer circuit shown in Fig. 3. $I_{\rm IN}$ and $I_{\rm O}$ are the input currents and $I_{\rm OUT}$ is the output current. KCL and KVL result in (1) and (2), respectively.

$$I_{\rm OUT1} = 3I_{\rm IN} - I_O \quad (1)$$

$$V_{\rm GS1} + V_{\rm GS3} = V_{\rm GS4} + V_{\rm GS2} \quad (2)$$

Considering all transistors in the saturation region, ignoring body-effect and channel length modulation, and taking W/L ratios of $\mathrm{Q}_1, \mathrm{Q}_2, \mathrm{Q}_3$, and Q_4 to be the same, the expression

$$I_{\rm OUT1} = 4I_{\rm IN} - I_O - 2 \times \sqrt{(I_O \times I_{\rm OUT1})} \quad (3)$$

is derived from (2).

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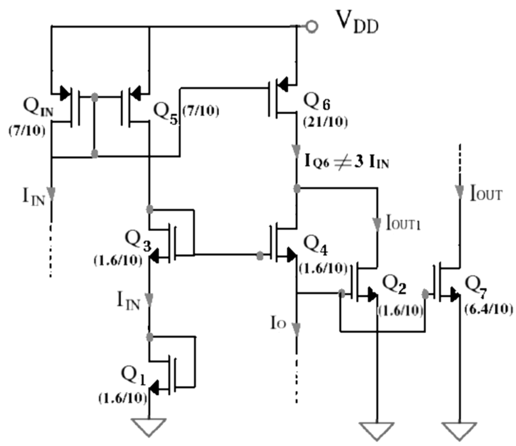

Fig. 3. Current-squarer circuit with proper I/O arrangement. Note: Numbers in brackets indicate the W/L ratios of all transistors in micrometers.

Replacing $I_{\rm OUT1}$ in (3) with the right side of (1) leads to

$$I_{\rm OUT1} = \frac{I_{\rm IN}^2}{4 \times I_O}. \tag{4}$$

Finally $I_{\rm OUT}$ is obtained by mirroring $I_{\rm OUT1}$ with a factor of 4, as given by

$$I_{\rm OUT} = \frac{I_{\rm IN}^2}{I_O}. \tag{5}$$

Note that (4) is obtained from two independent equations (1) and (3) used to describe $I_{\rm OUT1}$ as a function of $I_{\rm IN}$ and $I_{\rm O}$. For (1) and (3) to be true simultaneously, it follows that

$$I_{\rm IN}^2 - 12 \times I_{\rm IN} \times I_O + 4 \times I_O^2 = 0. \tag{6}$$

Equation (6) shows that $I_{\rm IN}$ and $I_{\rm O}$ cannot be independently applied to the circuit. The flaw in the analysis arises because two equations with two preassumed independent variables are used to describe $I_{\rm OUT1}$ in (4). In reality, if $I_{\rm IN}$ and $I_{\rm O}$ are independently applied to the circuit, the circuit satisfies (2) and (3), but not (1). Applying two independent current sources drives transistor $\rm Q_6$ into ohmic region causing $I_{\rm Q6}$ to be less than $3I_{\rm IN}$.

The circuit actually produces $I_{\rm OUT}$ as a nonlinear function of $I_{\rm IN}$, of which the details are given below.

Applying KVL results in

$$V_{\rm GS1} + V_{\rm GS3} = V_{\rm GS4} + V_{\rm GS7}. \tag{7}$$

Assuming $\rm Q_1, Q_3, Q_4$, and $\rm Q_7$ are all in saturation we have

$$I_{\rm OUT} = 16 \times I_{\rm IN} + 4I_O - 16\sqrt{I_{\rm IN} \times I_O}. \tag{8}$$

Equation (8) gives the real relation between $I_{\rm OUT}$ and $I_{\rm IN}$.

The current-squarer circuit as shown in Fig. 3 was simulated using a Mentor Graphics custom IC design tool set, in TSMC 0.18-μm CMOS process with $\rm V_{dd} = 2$ V. $I_{\rm O}$ and $I_{\rm IN}$ values have the same range of values as given in [1]. Fig. 4 shows the simulation results for $I_{\rm O} = 1\ \mu$A, and $I_{\rm IN}$ ranging from 0.2 to 2 μA. Values of $I_{\rm OUT}$ versus $I_{\rm IN}$, obtained from simulation, closely follow relation (8). Thus the relationship between $I_{\rm OUT}$ and $I_{\rm IN}$ is not simply quadratic. Therefore the proposed circuit module in Fig. 1 of [1] (also shown in Fig. 1 of this paper) does not behave like a current-squaring circuit.

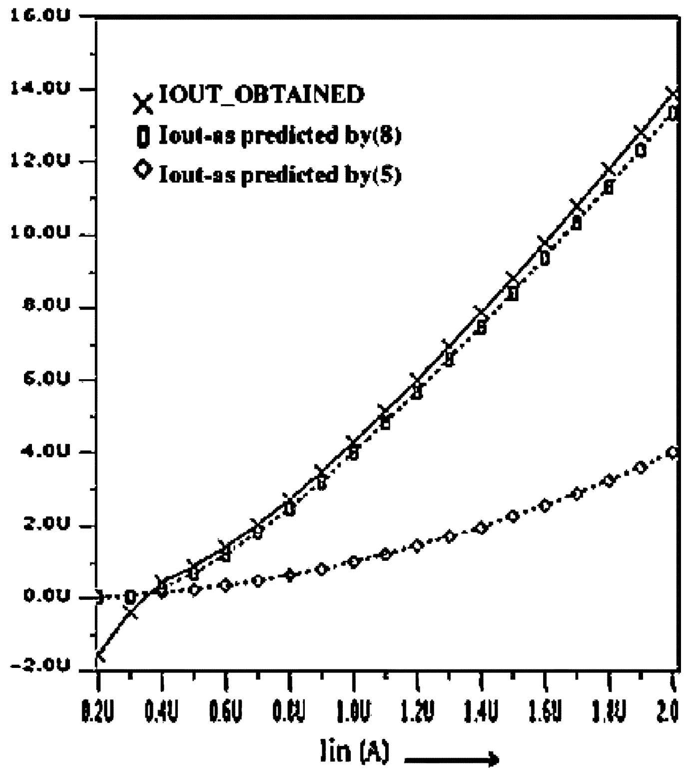

Fig. 4. Simulation results of the current-squarer circuit of in Fig. 3 (with $\rm I_O = 1$ uA).

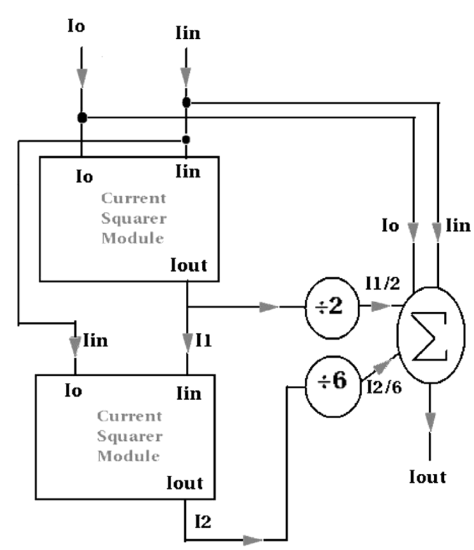

Fig. 5. Block diagram of pseudo-exponential function generator.

IV. Analysis of the Pseudo-Exponential Generator

Consider the pseudo-exponential generator produced using two current-squarer modules as building blocks in Fig. 5.

The expected value of $I_{\rm OUT}$ according to [1] is given by

$$I_{\rm OUT} \approx I_O \times \exp(I_{\rm IN}/I_O). \tag{9}$$

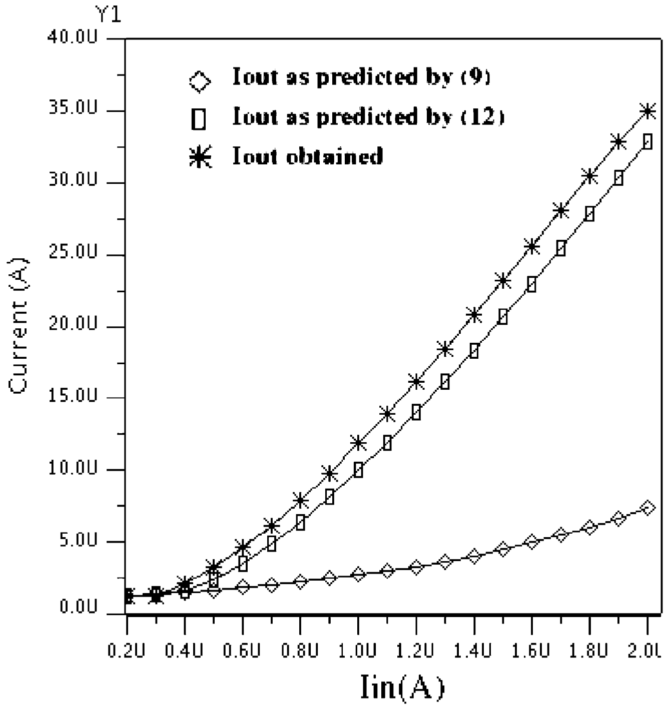

Fig. 6. Simulation results of the pseudo-exponential generator circuit ($\mathrm{V_{dd}} = 2$ V and $\mathrm{I_O} = 1$ uA).

However the actual value of $I_{\rm OUT}$ is derived as follows. From (8) we get

$$I_1 = 16 \times I_{\rm IN} + 4I_O - 16\sqrt{I_{\rm IN} \times I_O} \tag{10}$$

$$I_2 = 16 \times I_1 + 4I_{\rm IN} - 16\sqrt{I_1 \times I_{\rm IN}} \tag{11}$$

$$I_{\rm OUT} = I_O + I_{\rm IN} + \frac{I_1}{2} + \frac{I_2}{6}. \tag{12}$$

Fig. 6 shows the simulation results of the pseudo-exponential function generator circuit, produced using the current-squarer modules of Fig. 3 as building blocks. Simulation results confirm that $I_{\rm OUT}$ does not have an exponential relationship with $I_{\rm IN}$, and hence the pseudo-exponential function generator circuit proposed in [1] does not work correctly.

ACKNOWLEDGMENT

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REFERENCES

[1] C. Popa, "Improved accuracy pseudo-exponential function generator with applications in analog signal processing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 16, no. 3, pp. 318–321, Mar. 2008.